REMARKS

In the Final Office Action, the Examiner noted that claims 1 and 21-39 are pending in the application and that claims 1 and 21-39 are rejected. By this response, claim 1 is amended. In view of the above amendments and the following discussion, Applicants respectfully submit that none of such claims are obvious under the provisions of 35 U.S.C. §103. Thus, Applicants believe that all of these claims are now in condition for allowance.

Rejection of Claims Under 35 U.S.C. §103

The Examiner rejected claims 1 and 21-39 as being unpatentable over Bowen (U.S. Published Patent Application 2003/0105620, published June 5, 2003) in view of Smith et al., "An Architecture Design and Assessment System for Software/Hardware Codesign," IEEE, 1985, pp.417-424 ("Smith"). The rejection is respectfully traversed.

More specifically, the Examiner conceded that Bowen does not teach a step of invoking results of the traversing step using a high-level synthesis compiler to generate a functionality graph and a resource graph for the target architecture. (Final Office Action, p. 3). The Examiner stated, however, that Smith teaches production of a functionality graph and a resource graph. (Final Office Action, p. 3). The Examiner concluded that it would have been obvious to modify the hardware architecture program development of Bowen with the functionality and resource graphs taught by Smith. (Final Office Action, p. 3).

Bowen generally teaches writing first computer code in a first programming language (e.g., Handel-C), where the first computer code references second computer code in a second programming language (e.g., EDIF, VHDL). The second computer code is simulated for use during the execution of the first computer code in the first programming language. (See Bowen, Abstract; Claims 1-20). The Examiner specifically cites paragraph 0145 of Bowen, which generally describes the use of Handel-C to program FPGAs. The Examiner also cites paragraph 0268 of Bowen, which states that a compiler processes Handel-C code to produce a file, which in turn is compiled into native PC code using Microsoft Visual C++.

Smith generally teaches a CAD system that supports the codesign of hardware and software architectures for digital signal processors based on directed graph methodology. (Smith, Abstract). The CAD system employs a software graph to represent the software portion of the design and a hardware graph to represent the hardware portion of the design. (Smith, p. 421-423). The graphs are created by a designer and analyzed by the CAD system to assess performance. (Smith, p. 419-420).

Applicants have amended claim 1 to further clarify the invention. In particular, the intermediate graph representation stores features and characteristics of the plurality of hardware resources and interconnects between the plurality of hardware resources. (See, e.g., Applicants' specification, p. 20, lines 1-23). Moreover, claim 1 has been amended to recite mapping application code onto the plurality of hardware resources using the functionality graph and the resource graphs. (See, e.g., Applicants' specification, p. 8, lines 11-20; p. 29, line 23 through p. 30, line 15).

The cited references, either singly or in any permissible combination, do not teach, suggest, or otherwise render obvious Applicants' invention recited in amended claim 1. First, the combination of Bowen and Smith does not teach or suggest generating an intermediate graph representation that stores features and characteristics of a plurality of hardware resources and interconnects between the plurality of hardware resources. Compiling a file with Microsoft Visual C++, as taught by Bowen, does not teach or suggest generating an intermediate graph representation that stores features, characteristics, and interconnects associated with hardware resources. Smith generally describes use of directed graphs to represent software and hardware portions of a design. Smith does not teach or suggest generating an intermediate graph representation from an RDL description, as recited in Applicants' claim 1. Since neither Bowen nor Smith teach or suggest the intermediate graph representation as recited in Applicants' claim 1, no permissible combination of Bowen and Smith renders obvious Applicants' claim 1.

Second, the combination of Bowen and Smith does not teach or suggest mapping application code onto the plurality of hardware resources using the functionality graph and the resource graphs. Bowen does not teach or suggest

generation of functionality and resource graphs and thus does not teach or suggest use of such graphs. Smith describes use of directed graphs to represent software and hardware portions of a design. Smith does not teach or suggest using these directed graphs to map application code onto hardware resources of a target architecture. Since neither Bowen nor Smith teaches or suggests mapping application code onto hardware resources of a target architecture using functionality and resource graphs, no permissible combination of Bowen or Smith renders obvious Applicants' invention recited in claim 1.

Claims 21-39 depend, either directly or indirectly, from claim 1 and recite additional features therefor. Since the cited references do not render obvious Applicants' invention as recited in claim 1, dependent claims 21-39 are also nonobvious and are allowable. Accordingly, Applicants contend that claims 1 and 21-39 are nonobvious over the combination of Bowen and Smith and, as such, fully satisfy the requirements of 35 U.S.C. §103. Applicants respectfully request that the present rejection of such claims be withdrawn.

CONCLUSION

Thus, Applicants submit that none of such claims are obvious under the provisions of 35 U.S.C. §103. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring the maintenance of any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Justin Liu at (408) 879-4641 so appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on October 30, 2007.

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Name

KS to
Signature